## 24.6 A 16Gb/s Source-Series Terminated Transmitter in 65nm CMOS SOI

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The quest for high data rates at low power consumption and area has renewed interest in the source-series terminated (SST) driver. While SST drivers may not necessarily boast better performance than their counterparts using CML output stages, their advantage lies in their potential for lower power operation [1] and their ability to cope with a large range of termination voltages, which makes them a prime candidate for multi-standard TX. Given the increasing challenge in achieving acceptable analog performance in advanced digital CMOS technologies, the SST driver principle is based entirely on digital switching devices that are optimized for high-speed operation and continue to scale with technology. In this paper, the architecture and design of key components of a half-rate SST TX is presented that implements a versatile, power- and area-efficient equalization and impedance-tuning scheme. Furthermore, it achieves low jitter and negligible duty-cycle distortion (DCD), thanks to a clock duty-cycle cleanup circuit.

Figure 24.6.1 shows a block diagram of the implemented differential half-rate SST TX. All local clocks are derived from a global half-rate CML clock (ck2cml) and are converted to CMOS half-rate (ck2) and quarter rate (ck4) clock, respectively. The 4b quarter-rate input data d[0:3] is transformed in a first multiplexer stage to a half-rate interleaved even and odd data stream. Both even and odd data streams then pass a 4b shift register, that consists of 4 latches driven on opposing clock phases of the half-rate clock (ck2) and implements the delayed data taps of a 4-tap FIR pre-emphasis filter (tap[0:3][even, odd]). In order to set the sign of any pre-emphasis filter tap, each shift register latch output is followed by an XOR gate that selectively (sign[0:3]) inverts the corresponding filter tap. The resulting 4 even/odd (=8) half-rate tap data streams, along with the half-rate CMOS clock ck2, are then globally distributed to 44 identical differential half-rate SST driver slices, each of which can be configured to select one even/odd tap stream out of the available 4×2 tap data streams. Consequently, each SST driver slice can be assigned to any of the 4 FIR taps, which adds versatile power- and area-efficient equalization capabilities to the TX.

Figure 24.6.2 depicts a schematic of a half-rate differential SST slice. Each slice is composed of 2 single-ended SST drivers to form a pseudo-differential output stage. One single-ended slice contains 2 pull-up/pull-down branches with the corresponding even and odd data and select transistors, along with a common pull-up/pull-down polysilicon linearization resistor. Even and odd data for both single-ended SST slices are derived from two 4:1 input multiplexers to select the data stream corresponding to the assigned FIR position. In order to guarantee stable data and the appropriate timing at the multiplexing output SST stage re-timing latches are introduced. Note that the output impedance of the driver is equal to the parallel combination of all the SST slices, and it does not matter whether a particular slice is pulling up or down. Termination-impedance tuning is obtained by some additional logic to disable a certain number of SST slices and to set them into high impedance (enable=0). A nominal 50Ω impedance is achieved when 30 SST slices are enabled, leaving a tuning range of ±14 slices to comfortably cope with process tolerances. A MOS to poly resistance ratio of 1:3 is chosen in this implementation for optimum accuracy/area trade-off.

A particular concern in a half-rate SST TX lies in the fact that it operates at both clock cycles of the half rate CMOS clock ck2 and any imbalance or DCD has a direct impact on the jitter performance. Special measures are taken in the CML-to-CMOS clock converter, shown in Fig. 24.6.3(a), to cleanup DCD. The first CML buffer stage uses DC suppression and acts as a first DCD-cleanup stage [2]. In addition, it provides some gain to maximize the CML output signal swing (out, outb). An AC-coupled inverter with resistive feedback then follows the first CML buffer and acts as a CML to CMOS conversion stage [3]. AC-coupling is a simple and efficient way to remove any DC component and to perform a voltage level shift to the input of the inverter, which is DC biased to its trip point by means of the feedback resistor. Three tapered CMOS inverters then follow to provide enough drive strength to globally distribute the half-rate CMOS clock ck2/ck2b to the 44 unit SST slices. Care is taken to minimize delay (~ 43ps) in the CMOS clock path for minimum power-supply-noise-induced jitter. Furthermore, special attention is paid in the circuit layout to keep the fully differential clock nets ck2/ck2b symmetrical.

A circuit layout of the implemented SST TX is shown in Fig. 24.6.3(b). The macro occupies an area of 230×56μm² including ESD protection. In order to characterize the performance of the SST TX, a wafer probable test chip is implemented (Fig. 24.6.4). The test chip consists of 2 SST TX lanes that share a common external differential half-rate CML clock input. A serial 3-wire interface allows control of the TX settings and the 2 bit-pattern generators that generate independently programmable quarter-rate data for both TX lanes. Furthermore, supply decoupling capacitors in the order of 50pF/lane are added closely to each TX lane. A chip micrograph is shown in Fig. 24.6.7.

Figure 24.6.5 shows 3 measured PRBS15 differential data eyes at 16Gb/s data rate and at 3 different termination voltages Vtt, along with the measured jitter numbers. Sub-ps RJ is measured, which is essentially at the resolution limit of the measurement equipment, while the measured DJ is ~8.5ps and dominated by ISI. Split wafer lot measurements of DCD at data rates between 5.2 to 12.5Gb/s remain below 600fs. A DC jitter supply sensitivity of -4.6ps/100mV (@$V_{dd}$=1V) could be observed. Only a slight degradation in DJ of <1ps could be observed when switching the neighboring lane in operation. No perceivable difference in the jitter performance nor in the eye opening could be observed for any termination voltage Vtt from 0 to 1V, which proves the versatility of the SST TX to cope with different termination standards. The quality of the SST TX clocking path is not only confirmed by sub-ps RJ, but also with the DCD-cleanup performance. Figure 24.6.6 shows the measured output peak-to-peak DCD versus an incoming-clock DCD at a data rate of 5Gb/s (2.5GHz CML clock) and different termination voltages Vtt. The measured output DCD at all termination voltages remains below 0.5%pp at an input DCD of ±10%. The measured supply current of one SST TX lane including bit-pattern generator at 16Gb/s and differential 100Ω termination is 57.5mA at a nominal $V_{dd}$ of 1V, corresponding to a power-dissipation efficiency of 3.6mW/Gb/s.

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*References:*
[1] H. Hatamkhani, K. J. Wong, R. Drost, et al.,"A 10mW 3.6Gbps I/O Transmitter," *Symp. VLSI Circuits*, pp. 97 - 98, Jun., 2003.
[2] C. Menolfi, T. Toifl, R. Reutemann, et. al, "A 25Gb/s PAM4 Transmitter in 90nm CMOS SOI," *ISSCC Dig. Tech. Papers*, pp. 72-73, Feb., 2005.
[3] J. Savoj, B. Razavi, "A CMOS Interface Circuit for Detection of 1.2Gb/s RZ Data," *ISSCC Dig. Tech. Papers*, pp. 278 - 279, Feb., 1999.

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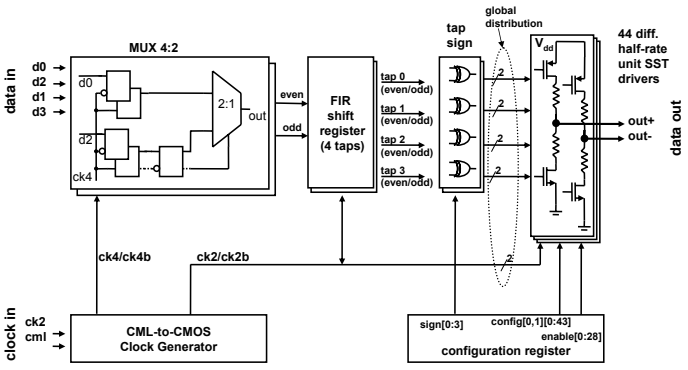



Figure 24.6.1: Half-rate SST TX block diagram.

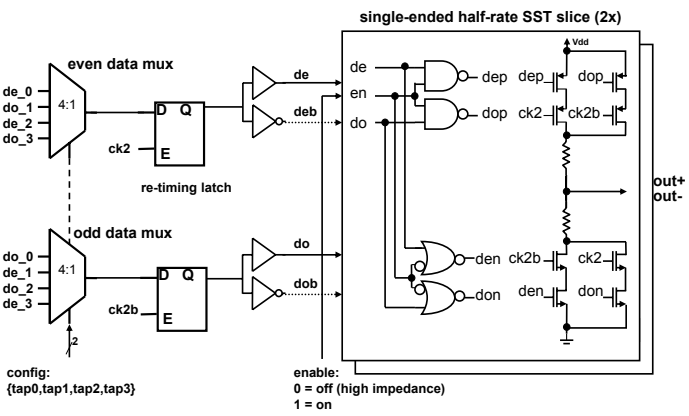



Figure 24.6.2: SST driver half-rate slice architecture.

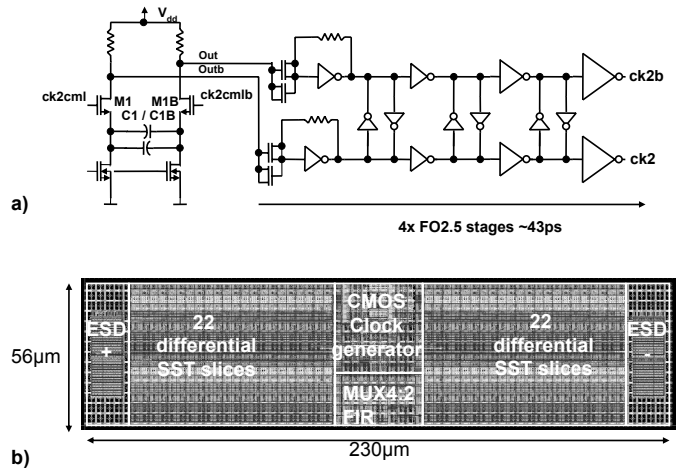



Figure 24.6.3: (a) CML to CMOS converter with DCD cleanup, (b) Layout of one SST TX core.

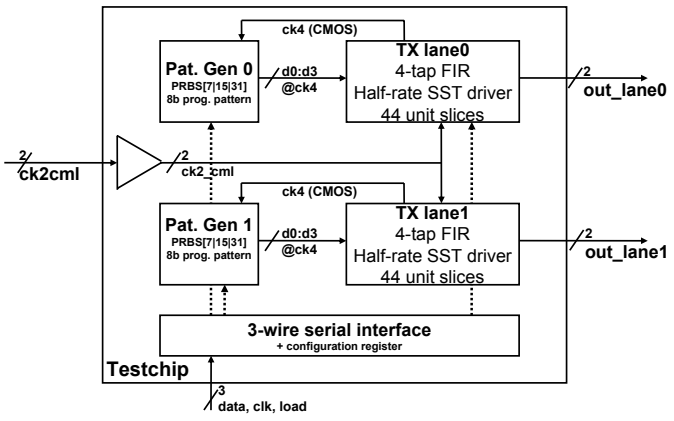
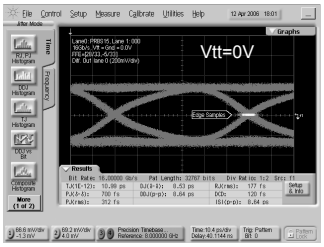
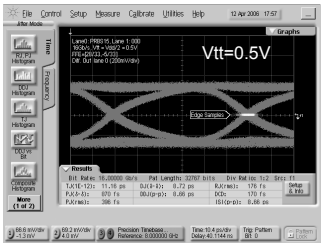
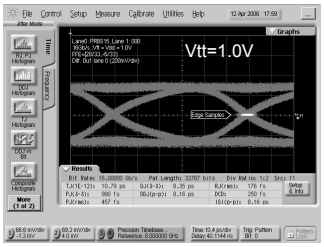



Figure 24.6.4: Test-chip block diagram.

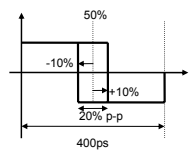



| 16Gb/s, PRBS15 | RJ [ps] rms | DJ(d-d) [ps] | DCD [ps] | TJ [ps] (BER 1e-12) |
|---|---|---|---|---|
| Vtt=0V | 0.177 | 8.53 | 0.120 | 10.99 |
| Vtt=0.5V | 0.176 | 8.72 | 0.170 | 11.16 |
| Vtt=1.0V | 0.176 | 8.35 | 0.250 | 10.79 |

Figure 24.6.5: Measured PRBS15 data eye at 16Gb/s and at different termination voltages Vtt.




Applied input clock signal @ 2.5GHz

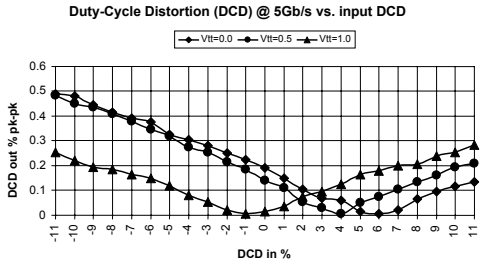



Figure 24.6.6:Measured output DCD versus input-clock DCD at 5Gb/s and different termination voltages.

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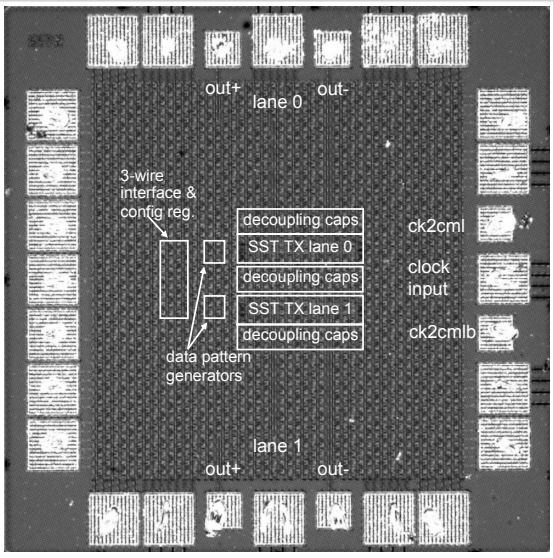


**Figure 24.6.7: Test-chip micrograph.**

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